SimpliPHY
Copper PHY Bring Up Guide

Application Note

Subject to Change

AN0155

Revision 01–00

15 Jan 2007

Confidential

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Document History

The following table lists the history of this document.

Table 1 Document History

Revision	Date	Description
01-00	15 Jan 2008	Initial Document Release

1 Introduction

This document provides useful guidelines for hardware and software engineers bringing up a SimpliPHY gigabit copper PHY for the first time on their prototype board. It is geared toward speeding development to production.

1.1 References

1.1.1 Vitesse Documents

- Vitesse Copper PHY Datasheets
- Vitesse Copper PHY Design and Layout Guides

1.1.2 IEEE Standards

- IEEE802.3, CSMA/CD Access Method and Physical Layer Specification

1.1.3 External Documents

- High Speed Digital Design, Author: Howard Johnson, PH.D., ISBN 0-13-395724-1

2 Designing with SimpliPHY Devices

Vitesse wants to thank you for taking the opportunity to design with one of the most innovative Ethernet PHY devices in the market. Originally Cicada Semiconductor, which was acquired by Vitesse Semiconductor in 2004, the mission of the Gigabit Ethernet PHY design team is to continually innovate the industry with system integration of passive components, best energy efficiency practices to achieve the industry's lowest power PHYs in production, and also provide innovative features for testability purposes. This document outlines the steps a hardware/software designer needs to take to bring a Vitesse copper PHY to full functionality.

2.1 Design Documentation

Vitesse recognizes that a designer can only achieve the best designs with the most recent available documentation. We make a practice of continually ensuring our online documentation is the most up-to-date with all the datasheets and application notes you need to design for first pass success. As a result, even if one has designed with a Vitesse copper PHY before, it is advisable to visit the Vitesse website (http://www.vitesse.com) and analyze the specific product page to ensure you have the latest documentation.

Two of the most important documents a designer needs are the datasheet and the design and layout guide. The datasheet will provide the most in-depth information including:

- Functionality
- Register map
- Pin information
- Electrical specs

The Design and Layout Guide is an additional document that highlights commonly used design practices to achieve first pass success. It will include information such as:

- Grounding
- Power considerations
- Thermal considerations
- Copper/Fiber interface
- MAC interface
- Other miscellaneous design information

These two documents provide information to help you with your design. In addition, Vitesse is more than willing to also review your schematic. When you are ready, contact your local Vitesse sales/distribution representative and arrange a schematic

review for your design. While not required, to ensure an accurate review, please make sure to provide the following:

- Device used (if not obvious in the schematic)
- If the PHY is being used in an a-typical manner, please provide a block diagram/description to help us ensure we are correctly reviewing your innovative application.
- Magnetic part number. If the device is not found on the web, please forward the datasheet along with the schematic
- If not obvious in the design, what the MAC interface of the PHY is connected to.
- The origination points of the JTAG, MDC/MDIO, and Clock inputs
- Resistor values (if not already listed)
- Do not install (DNI) list if not apparent in the design
- Power being applied to the power supply pins

The next section will describe the first steps to bringing-up the copper PHY device for the very first time.

3 1st Steps for Bringing-up the PHY

Once you receive your completely assembled proto-type boards with a SimpliPHY device included, it is highly recommended one follows these first steps to avoid many headaches involved with bringing up a copper PHY device for the first time.

3.1 Board Inspection

The first step is to visually inspect the board to ensure that all components placed are correct, in the proper oriented location, and there are no cold or missing solder joints on both the PHY device and its associated devices (recognizing that this step is difficult with BGA devices).

3.2 First Power-Up

The next step is to power up the device. This involves powering up all power rails associated with the PHY. While all SimpliPHY devices to not have power sequencing, it is still advisable for reliability to power all supplies in a relatively simultaneous manner. At this stage, for the first power-up, it is advisable to measure the design's power network and ensure that all power supplies are correctly set to the correct voltage for all rails. The best place to measure is either at the pins of a QFP or at the decoupling capacitors underneath the BGA closest to its power pins.

Each Copper PHY has three supply rails: 3.3V, 1.2V, and 1.2V filtered analog that connect to the power pins of the device. Note that the VSC8211/21 and VSC8224/44 have an additional 3.3V filtered analog. This is an important step because inadequate power supplies cause the most common cause of link failures, auto-negotiation problems, and random system event such as CRC errors. At some point during full system data traffic testing, it is also advisable to check these power supplies again to ensure the local decoupling network is supplying a proper voltage to these pins at all times and is capable of filtering out the transient responses that occur during data traffic operation.

3.3 Clock and Reset Inspection

After the first power-up, the next step is to check the PHY input clock and reset. Power must be applied and the clock (either 25MHz or 125MHz) must sending pulses at the correct frequency for the prescribed period of time in the datasheet before the reset pin (or pins in the case of devices with soft_reset) is released. In the event of a power or clock loss, the reset must be re-applied in order to bring the device back to a known operational state. To ensure the device will properly respond to the clock, the PLLMODE and OSCEN pins must be set correctly based on the type of clock input. For example: a 25MHz TTL input requires the PLLMODE = 0 (low) and OSCEN = 0 (low).

At this point, plugging in a cable with a working link partner on the other end should achieve a link-up. If this does not happen, please go to the next section which describes a few trouble-shooting steps to help determine the problem

4 Troubleshooting

There are two types of basic bring-up issues:

- No link-up
- Link-up but no traffic passing or CRC errored traffic

The following sections will help guide the user to locate the problems preventing normal operation. Please feel free to contact your Vitesse technical support engineer to assist you with this process.

4.1 DC Board Level Measurements

While a Gigabit Copper PHY is a very complex device, a normal operating PHY will still have specific visible behaviors that can be observed with basic lab measurement tools. As an example, many of these can be measured with a DC volt-meter. Here is what to examine once power has been applied, reset is deasserted, and a clock is being provided to the device.

If the power is up and stable, the following can be seen:

- REF_FILT pin = ~1.15 to ~1.25 VDC

- REF_REXT pin = ~0.98 to ~1.06 VDC
- Copper Pair A and B = ~1.65 VDC

Problems in this area usually are related to power and grounding issues. The Copper pairs' voltages are set by halving the VDD33 voltage supply (3.3 V / 2 = 1.65 V)

4.2 Oscilloscope Board Level Measurements

In addition, several areas of the device can be examined with a basic oscilloscope. When reset is deasserted and a clock is being provided to the device, the following can be seen:

- Copper Pair A and B = You should see link pulses and they should alternate between A and B (which is the Auto MDI/MDI-X operation happening)
- Copper Pair C and D = No link pulses present. In the absent of a link partner, this is normal as auto-negotiation only works on pairs A and B. During normal operation these pins are only used for 1000BASE-T and not used in 10/100BASE-T
- MDC/MDIO = One should see clear pulses if the host is trying to communicate with the PHY. Use the read command to see if the PHY responds after the Turnaround bit.
- CLKOUT = if enabled, you should have a 125MHz output which means the internal PHY PLL is operational.

Problems with any of these items can be related to several issues. The obvious one is a subtle power issue. Also, it is important to ground the JTAG TRST pin when in normal operation and releasing the PHY reset. The copper PHYs do not have an internal power-up reset circuit for the JTAG and as a result, this must be handled via the JTAG TRST in order to configure the boundary scan chain to a known state. This issue manifests itself as unreliable linkups after several resets (works sometimes, but not always after reset is deasserted). Problem related to MDC/MDIO could be improper impedance traces or improper board termination (the MDIO requires a pull-up at some point along the trace as this signal is open drain).

If designing with an RGMII interface, it is important to check to make sure that the proper delay line compensation is set correctly. Usually what can be done is to measure one side of the RGMII path's clock, the CTL pin and one of the data pins. If it is assumed the transmitter is providing the delay, then this should be seen via this measurement. If the delay is taken care of at the receiver, then the clock, data, and control pins should all line up. Any skew within this measurement could be the reason why CRCs or no data is being passed.

4.3 Register Level Measurement

If no data is being passed or CRC are present, it is important to isolate the problem. This can be done with register settings. First step is to discover from where is the source of the problem. One general rule to consider is that a packet that traverse through a PHY can either be interpreted as a good packet, a bad (CRC) packet, or a dropped packet. Generally, MACs drop errored packets in the ingress side and egress

errored packets are captured as CRC errors by test equipment and PHYs that can detect CRCs. This is not always the case, but can help guide one to discover the root of the pathway issues.

4.3.1 RJ45 to the PHY Ingress Path

To debug if this pathway is working: ensure that the link is up, the link partner is actually providing traffic, and read the local PHY's CRC counters and verify that the packets are being counted. If the link partner sends 100 packets, the local PHY's counter should increment the counter by 100. If not, see if any of these good packets are being interpreted as CRC packets via this counter. The PHY cannot drop a packet. If a fragment is being processed by the PHY, it will continue to pass this along and count it as a packet where as a MAC may just drop it.

4.3.2 PHY to RJ45 Egress Path

There are several ways to determine if this path is valid. First, is to have the MAC transmit a set number of packets and count them at the link partner. If this is not possible, the Copper PHY has a packet generator. This can be enabled and the link partner can be used to determine if the packets were actually transmitted. Combining this pathway to the previous one, the far-end loopback can be used and one could have the link partner transmit packets and the link partner then captures the incoming packets to determine if they actually made it to the PHY and returned.

4.3.3 PHY to MAC Pathways

Among the most common problems of pathway issues, the majority occurs between the PHY and the MAC due to impedance or timing skew issues. The steps in the previous two sections can be used here as well to help isolate the problem. For example, a packet generated by the link partner, to the PHY, and bound for the MAC, counted by its counter. If this packet is errored, it will likely be dropped. In certain cases, it may make sense to use the near-end loopback to help isolate issues. In some cases, customers may have gotten the TX and RX backwards or even the + and – signals for SGMII in the wrong orientation.

4.3.4 Miscellaneous Issues

Other issues that one can troubleshoot are to ensure that all relevant advertisements in Register 0, 4, and 9 are set properly. Also, the operating mode in Register 23 is configured correctly for a particular media interface. Auto MDI/MDI-X should be properly configured, as well. Some PHYs require an initialization script for normal operation. Please refer to the associated device datasheet and design and layout guide for more information.