Introduction

The purpose of this application note is to provide specific design and layout guidelines to printed circuit board and software designers utilizing the VSC8221 physical layer device.

Power Supply Organization and Decoupling

The VSC8221 requires a 3.3V and a 1.2V power supply source for basic operation. The 1.2V power can be provided from an external power supply source or from the VSC8221's on-chip 1.2V switching regulator.

PCB Power Plane Organization

It is recommended that the PCB power plane(s) in a system be divided into separate regions:

Table 1: Power Supply Plane Regions

Plane Region	Description	Associated VSC8221 Power Pins
V+IO ($_{IO, MICRO, CTRL}$)	Input/output buffer supply(3.3V-2.5V)[a]	VDDIO ($_{IO, MICRO, CTRL}$)
VDD33A	Filtered analog 3.3V supply	VDD33A
VDDREG	3.3V power supply for on-chip switching regulator	VDDREG
VDD12A	Filtered analog 1.2V supply	VDD12A
VDD12	High-current digital core 1.2V supply	VDD12

a. This supply is used by three different I/O functions (IO, MICRO, and CTRL), each of which can operate at a different voltage. The V+IO region should be further divided depending on how many different operating voltages are used.

Power Supply Filtering and Decoupling

For best performance, each power supply region should contain capacitors for both bulk decoupling and for high-frequency local decoupling. This is summarized in the following table:

Table 2: Bulk Decoupling for the 100 TF-BGA

Power Supply Plane Region	Bulk Decoupling Required	Local Decoupling Required[a]
V+IO	1uF	3 0.1uF capacitor
VDD33A	10uF	3 0.1uF capacitors
VDDREG	1uF	1 0.1uF capacitor
VDD12A	1uF	1 0.1uF capacitor
VDD12	10uF	6 0.1uF capacitors

a. These numbers are based on typical performance of pre-production silicon at 25^{o}C operating in full-duplex 1000BASE-T mode.

Bulk decoupling capacitors should be sintered solid tantalum and can be placed at any convenient position on the board. Local decoupling capacitors should be placed as close to the VSC8221 as possible. The best location for local decoupling capacitors is on the bottom of the board, directly under the VSC8221 (see Figure 2 below)

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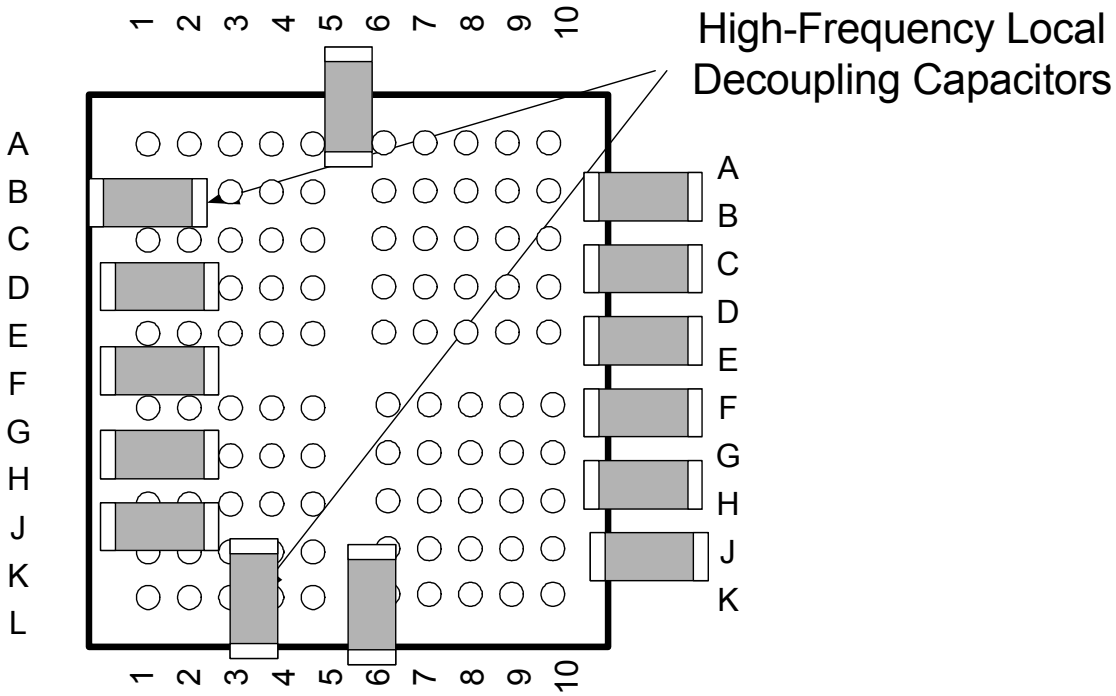


Figure 1: Local High-Frequency Decoupling Capacitor Layout
(View from top of PCB)

In addition, a ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.

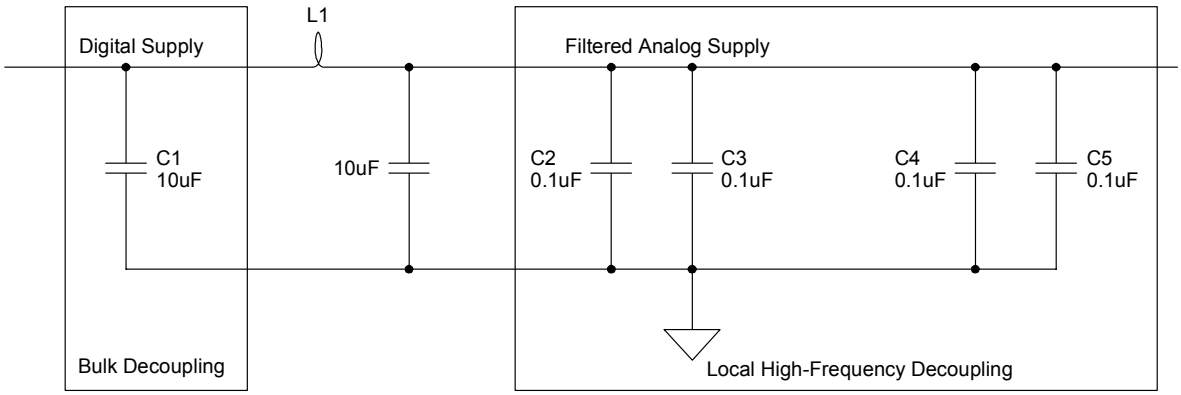


Figure 2: Decoupling Schematic

The beads should be chosen to have the following characteristics:

- Current rating of at least 150% of the maximum current of the power supply
- Impedance of 80 to 100Ω at 100MHz

Recommended beads are:

- Panasonic EXCELSA39 or similar
- Steward HI1206N101R-00 or similar

Since all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. For this reason, it is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors, once thorough evaluation of system performance is completed.

On-chip 1.2v Regulator

It is recommended that the on-chip 1.2V regulator be used as the source for the VDD12 and the VDD12A supplies. This is advantageous from a PCB space and cost perspective. The figure below shows the relevant PHY connections when the on-chip 1.2V regulator is used:

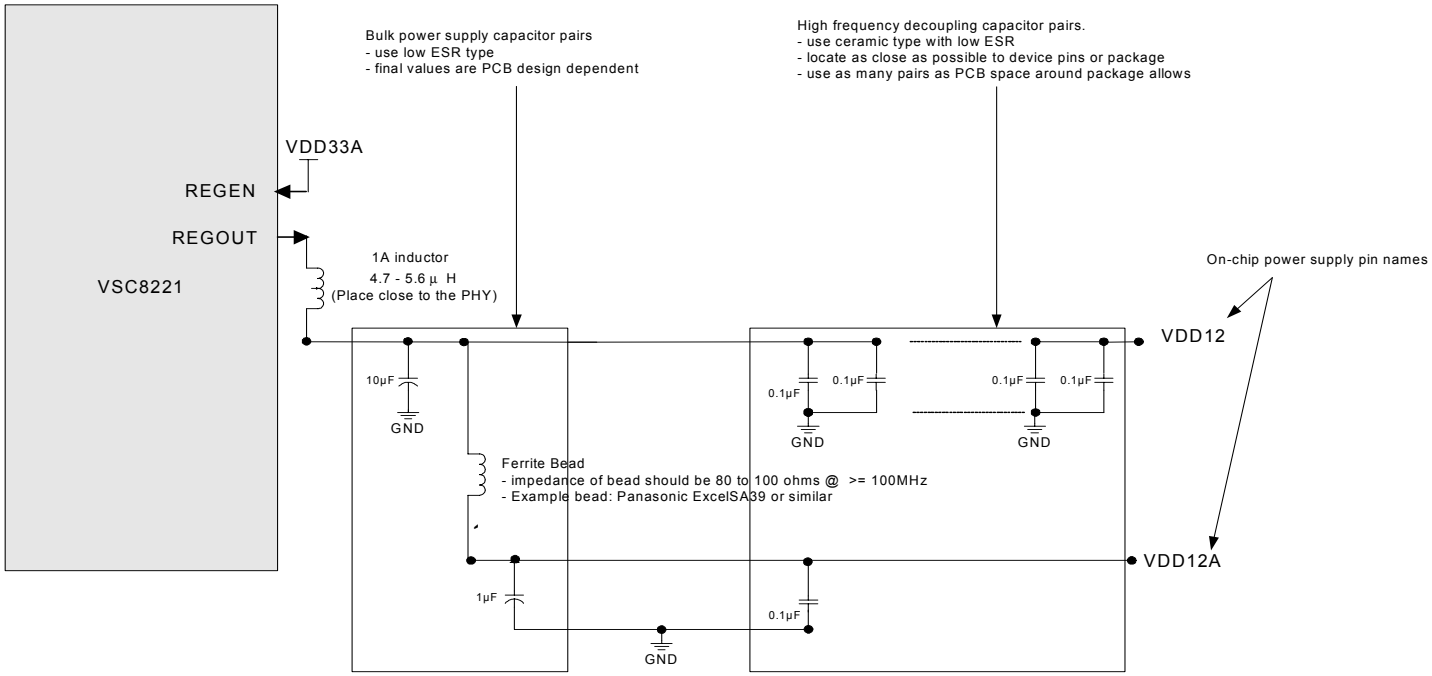


Figure 3: 1.2V Supply using on-chip Regulator

PCB Chassis Ground Region

To isolate the board from ESD events and to provide a common-mode noise ground path, a separate chassis ground region should be allocated. This should provide an electrical connection to the external chassis and the shield ground for RJ-45 connectors. In addition, the “Bob Smith” termination impedance should be connected between this ground and the cable-side center-taps of the magnetics modules. (see Figure 4: ”Ground Plane Layout” and Figure 5: ”PHY and Magnetics Circuit”, below

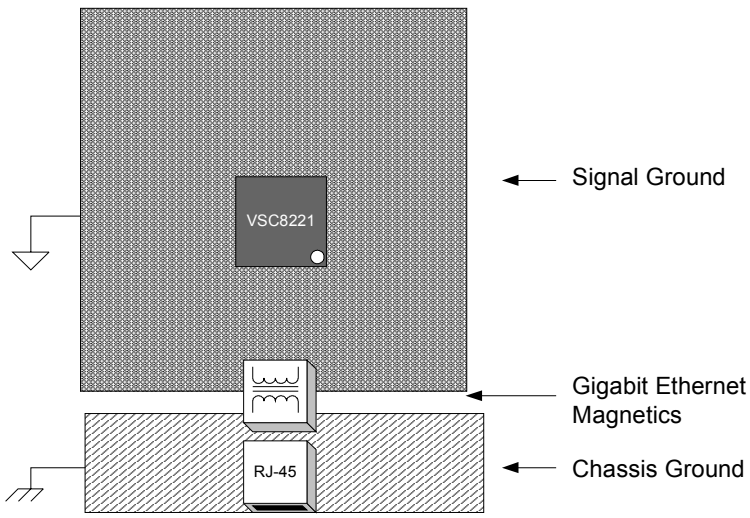


Figure 4: Ground Plane Layout

PHY Magnetics Connections

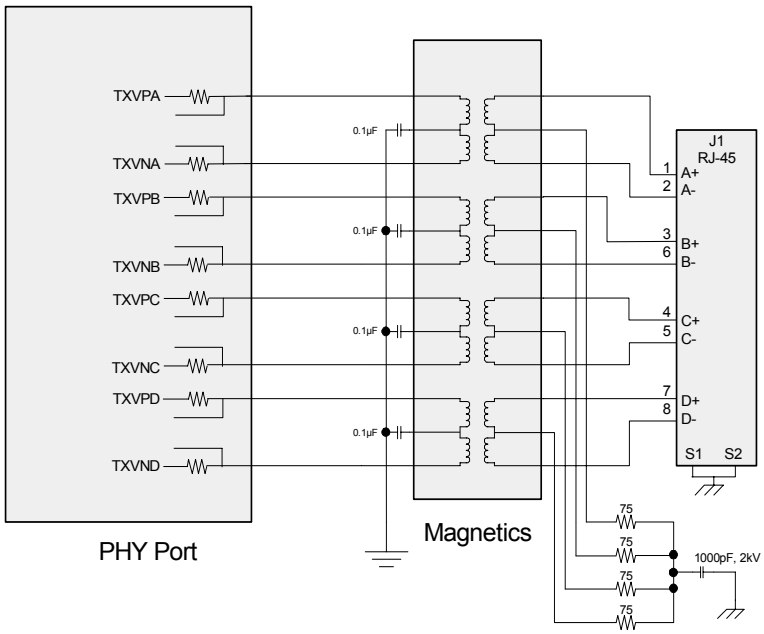


Figure 5: PHY and Magnetics Circuit

The magnetics shown in the above figure are available in different configurations. Each of the configurations has its advantages and dis-advantages. For details on magnetics refer the 'Magnetics and EMI control' application note.

As stated in section 6 'SimpliPHY'd Magnetics and EMI control for SFP applications' of the 'Magnetics and EMI control' application note a Type II configuration magnetics created using a small form factor BGA Type I magnetics and common mode chokes between the PHY and Type I magnetics is ideally suited for SFP applications from a EMI and PCB area stand point. The figures below shows the schematic of a Type II configuration magnetics built using a Type I magnetics and a ferrite bead. Refer to the VSC8221IMEV or the VSC8221HHEV reference SFP design kits for more details on the Layout.

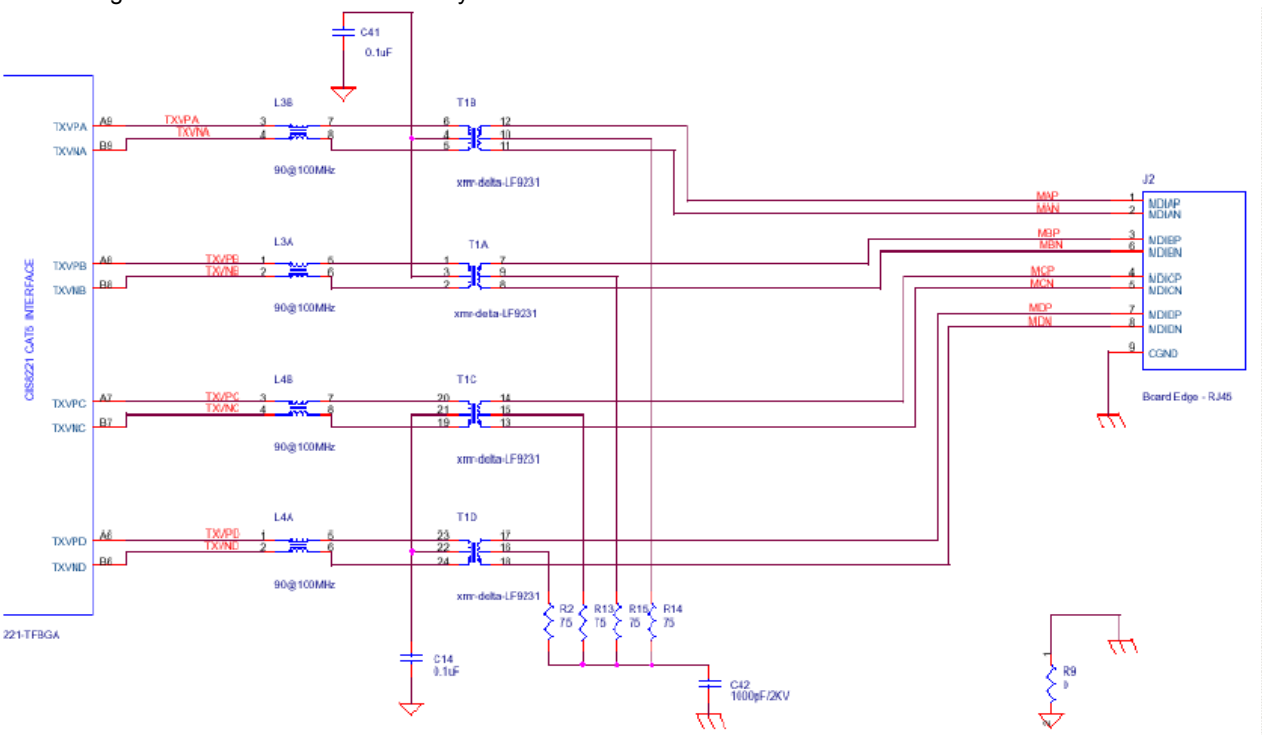


Figure 6: Reference Magnetics circuit for SFP Application

High Speed Serial Interfaces

Serializer/Deserializer (SerDes)/SGMII

Best performance will result when SerDes traces are placed using the following design rules:

Traces should be routed as 50Ω (100Ω differential) or 75Ω (150Ω differential) controlled impedance transmission lines (microstrip, or stripline).

Traces should be of equal length on each differential pair to minimize EMI and Jitter.

Traces should be run adjacent to a single ground plane to match impedance and minimize noise. If traces are placed between two ground planes to improve shielding note that this can cause problems if there is an impedance imbalance (noise) between the two planes.

Traces should avoid vias and layer changes.

A typical MAC PHY serial interface is shown below.

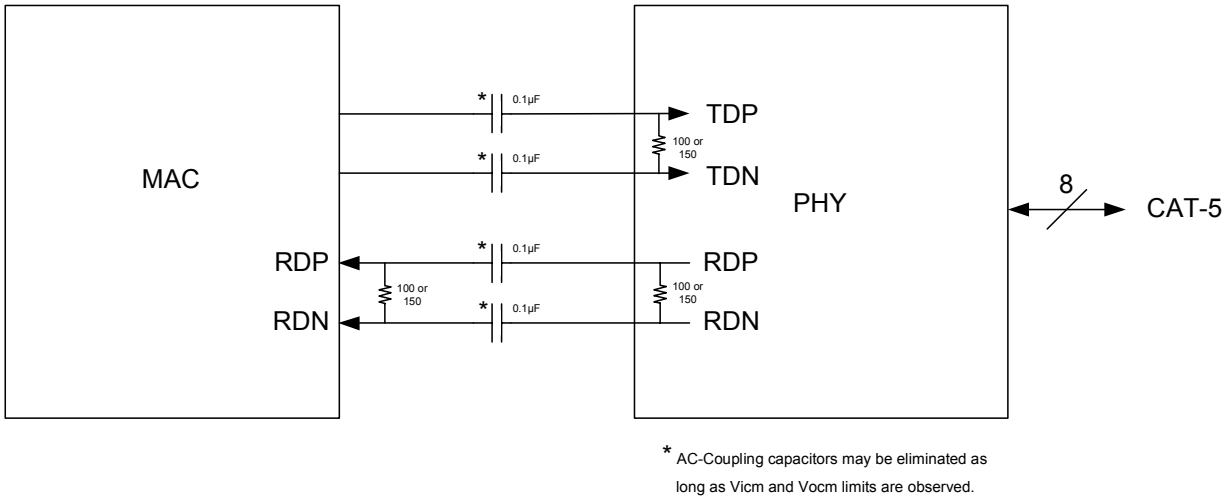


Figure 7: Typical MAC PHY Serial Interface

In general these connections require a series capacitor to prevent common mode voltages from interfering with transmit and receive operation. If the common mode input and output specifications for the MAC and VSC8221 are compatible (see data sheet section 'SerDes Specifications') then the series capacitors can be removed.

For example the VSC8221 Vicm min and max values would need to be equal to or wider than the matching Vocm specification for the MAC. Conversely the VSC8221 Vocm min/max range must fit inside the MAC Vicm range.

According to the SFP, MSA (Multi Source Agreement) specification, the above shown AC coupling capacitors must be on the SFP PCB.

Twisted-Pair Interface

These pins are the interface to the external CAT-5 cable and are organized in four differential pairs for each port. These are labeled "TXVPx" and "TXVNx", where 'x' is the particular pair within a single CAT5 cable. When routing these pairs on a PCB, the characteristics must match one of the following:

- Route each trace single-ended with a characteristic impedance of 50Ω referenced to ground.

--OR--

- Route each pair of positive and negative traces differentially, with a 100Ω differential characteristic impedance.

The VSC8221 PHY has internal termination for the twisted pair interface and does not need any external resistor on the traces connecting to the "TXVPx" and "TXVNx" pins.

Other Design Considerations

Design for Signal Integrity

With the high-speed nature of the VSC8221 data signals, careful attention must be paid to PCB layout and design to maintain adequate signal integrity. To simplify board design, the VSC8221 has been designed with SimpliPIN™ outputs on certain pins, which automatically calibrate their output resistance to 50Ω, eliminating the need for series termination resistors.

125MHz and 4MHz Clock Outputs

By default, the VSC8221 provides low-jitter, 125MHz and 4MHz output clocks for driving other devices in a system. The output resistance of these pins are self-calibrating to 50Ω, and should be routed on the PCB using a microstrip or stripline transmission line trace.

For each addition VSC8221 device in the chain, set PLLMODE to 1 by tying the EECLK/PLLMODE pin to VDDIOMICRO. This will enable each device to function using the 125MHz clock output of the previous device(s) in the chain.

Note that the clock outputs can be disabled by writing a '0' to MII register 18 and 17E, bit 0. Also the default 4MHz clock output of the CLKOUTMICRO pin can be changed to a 125MHz clock by setting extended MII Register 20E.8 to '1'.

An Important Note Regarding LED Outputs and JTAG TDO Pins

The LED outputs and JTAG TDO pins for the VSC8221 were designed with the same output driver technology as the high speed clock outputs above, which provide an extremely fast rise and fall time with integrated series termination resistors (see Figure 8: "Miscellaneous Series Termination", below). Even though the overall clock speed is much slower, these signals must be treated as high-speed signals to avoid reflections caused by the extremely fast transitions. This issue can be addressed in one of two ways:

- Route each signal using a microstrip or stripline transmission line trace with a characteristic impedance of 50Ω.
--OR--
- Ensure that the lengths of the PCB traces are less than 0.75 inches (approximately 19mm).

If the LED outputs are only driving LED devices and are not used with other digital devices, it is not necessary to route these traces as transmission lines, nor is it necessary to terminate them.

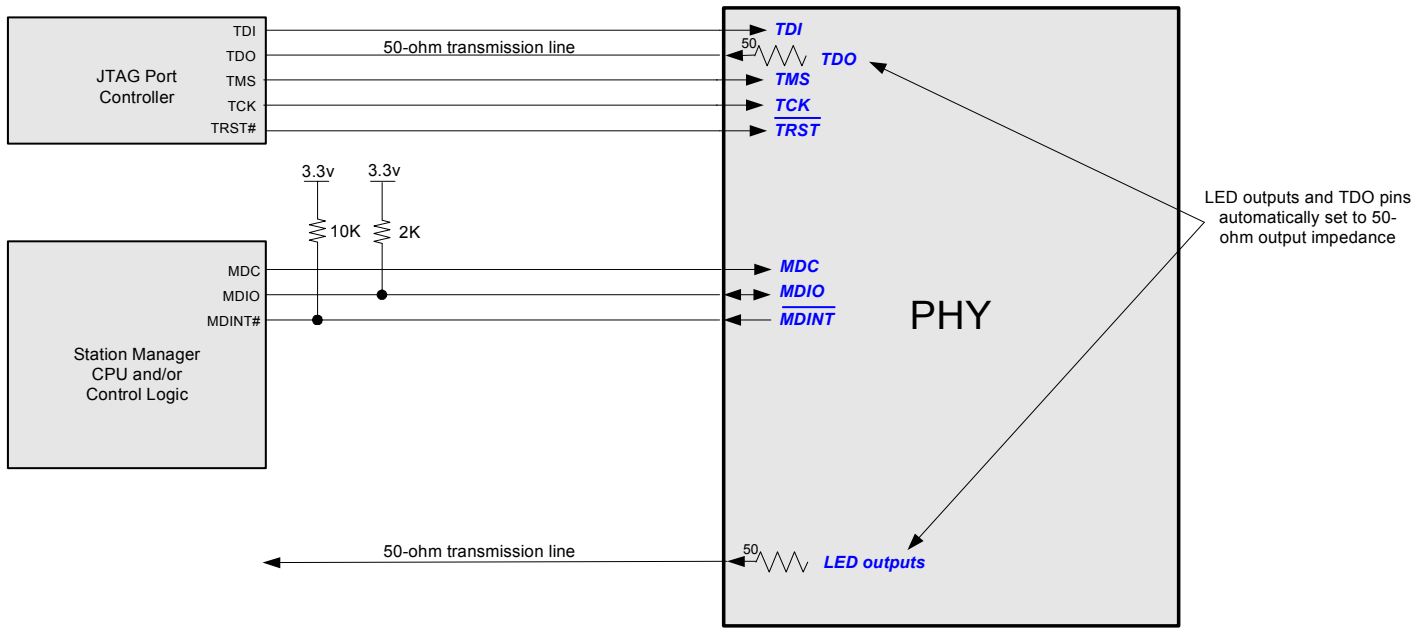


Figure 8: Miscellaneous Series Termination

RXLOS Behavior for SFP Application

The VSC8221 is set in SFP Mode when hardware configuration bit CMODE1.0 is set to ‘0’. In this mode the RXLOS/SIGDET pin drives the RXLOS output which is meant to be used as the source of the RXLOS signal pin of a standard 20 pin SFP connector as defined in the MSA specification. This RXLOS signal is an active high signal that is asserted whenever the CAT5 Media link is dropped. The precise behavior requirements of the RXLOS signal may be system dependent and therefore the VSC8221 provides programmability to the RXLOS behavior through MII Registers 30.1:0. This is described below:

Table 3: RXLOS behavior

MII Register 30.0:1 Setting	Behavior
00	RXLOS is always driven low.
01	RXLOS pulses (low-high-low) on a link down event for a period of 20ms.
10	RXLOS pulses (low-high-low) on a link down event for a period of 200ms.
11	RXLOS pulses (low-high-low) on a link down event for a period of 500ms.

RJ-45 Connectors and Magnetic Modules

RJ-45 Connector Recommendations

For system designers, several options exist for the choice of RJ-45 connectors. These are summarized as follows:

- Two tab orientations are available: up or down
- For multi-port connectors, two orientations are available: stacked and single-row.
- LEDs can also be integrated into the connectors.

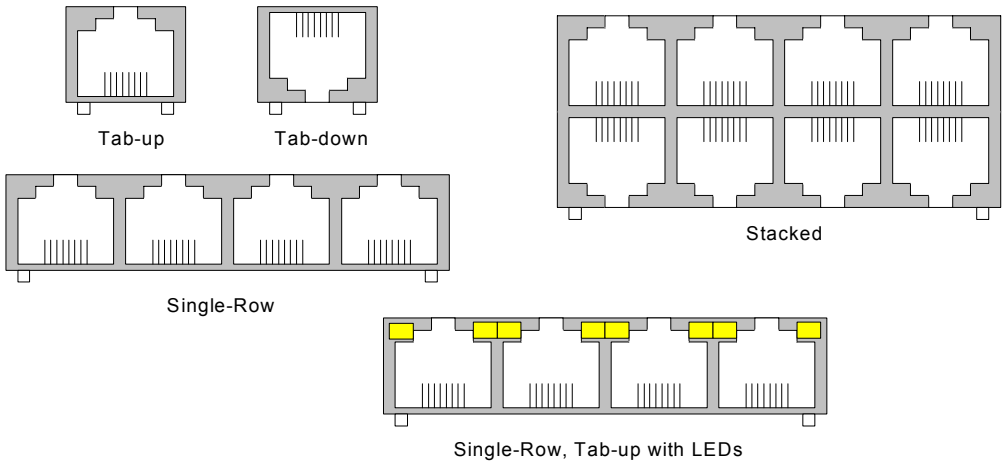


Figure 9: RJ-45 Example Configurations

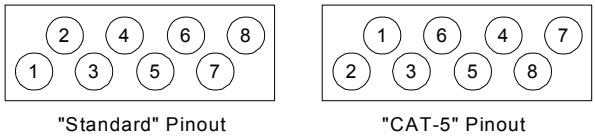
Most manufacturers can mix or match any combination of features. For example, LEDs can be added to any connector, or single-row multi-port configurations can be tab-up or tab-down. The exception is the stacked connector, which contains both tab-up and tab-down orientations.

An additional consideration is the pinout of tab-up versus tab-down connectors. The pinouts of these two orientations are reversed. While the VSC8221 will work equally well using either orientation, signal routing will be simpler with the tab-down pinout. For the stacked variety, both orientations exist in one package, so both pinouts typically exist in one package. Some manufacturers have provided an option for “vertical” pin orientation, which allows for ease in PCB routing.

CAT-5 vs. CAT-3 Connectors

When utilizing 1000BASE-T or 100BASE-TX, it is important that “CAT-5” RJ-45 connectors be used as opposed to “CAT-3”. This refers to the amount of crosstalk between the wire pairs within the connector.

In addition to the electrical characteristics, some manufacturers have two options for the connector pinout. These are typically labelled as “standard” and “CAT-5”. This is not to be confused with the electrical specification for the connector. Thus, two versions of a CAT-5 RJ-45 connector are available: one with a “standard” pinout and one with a “CAT-5” pinout:



Reset Sequence

The following events occur in order when the VSC8221 is brought out of reset. This is triggered by a low-to-high transition of the $\overline{\text{RESET}}$ pin.

1. Values for PLLMODE,EEDAT and CMODE pins are latched asynchronously immediately out of reset.
2. If the EEPROM is not present then on the first rising edge of REFCLK after reset, the SMI (Serial Management Interface) becomes active. Otherwise the SMI is disabled until the PHY configures itself using the initialization script loaded in the configuration EEPROM.
3. Approximately 11 milliseconds after reset, the reference voltages and currents stabilize.
4. Once a stable reference is available, the PLL requires 50 microseconds to lock.
5. With a locked PLL, the analog-to-digital converter is calibrated, which requires 2.05 milliseconds.
6. Once the ADC is calibrated, the clock outputs are activated

Important note: Since the values of PLLMODE and CMODE pins are latched on the rising edge of the $\overline{\text{RESET}}$ pin, it is required that the power supply is stable before the rising edge of $\overline{\text{RESET}}$. Therefore, if $\overline{\text{RESET}}$ is tied directly to a logic high on the PCB, the VSC8221 will behave unpredictably. If a design requires the $\overline{\text{RESET}}$ pin to remain high at all times, a small RC circuit can be added to this line to provide the necessary delay.

Also, note that the SMI is enabled prior to the other blocks within the device. For applications which utilize this interface, this sequence provides a short period of time in which to configure the VSC8221 before the device is fully operational. This is useful for setting up MII registers that control items such as LEDs, which must be setup prior to device operation.

Please refer to datasheet section ‘PHY startup and Initialization’ for more details on the reset sequence.

Thermal Performance

Though the low power consumption of the VSC8221 eliminates the need for external heatsinks or fans in most designs, certain guidelines must be followed for adequate heat dissipation. For proper operation of the VSC8221, a silicon junction temperature (T_j) equal to or below 125^{o}C must be maintained for commercial temperature ranges. Within the constraints of the commercial temperature range, the limits for junction-to-ambient thermal resistance are as follows:

$$\Theta_{ja(Commercial)} \leq \frac{T_j - T_a}{P_d} \leq \frac{125°C - 70°C}{1.1W} \leq 50.0°C/W$$

where Θ_{ja}=Junction to ambient thermal resistance, T_j = Junction temperature, T_a = Ambient temperature and P_d = Power dissipation.

For the purpose of maintaining adequate junction temperature, 21 balls in the center of the BGA package have been allocated for thermal relief. Each of these is connected electrically to VSS, allowing the use of PCB ground planes to transfer heat away from the BGA package. When utilized properly, these thermal balls can provide the necessary junction-to-ambient thermal resistance (Θ_{ja}).

For more information, please refer to the “Thermal Applications Data” section of the VSC8221 Data Sheet.

For proper cooling, a PCB via must be placed between the thermal BGA ball pads in a checkerboard pattern (see Figure 10: ”Thermal Via Layout”, below). Each of these “thermal vias” should then be routed to the BGA ball pads near it with a wide trace or solid copper fill to increase the conductive area on the surface of the PCB.

In order to dissipate heat below the BGA package, the PCB thermal vias must connect to a solid ground plane within the board. It is recommended that the ground plane have a minimum thickness of two ounces (see Figure 11: ”Thermal Ground Plane Connections”, below).

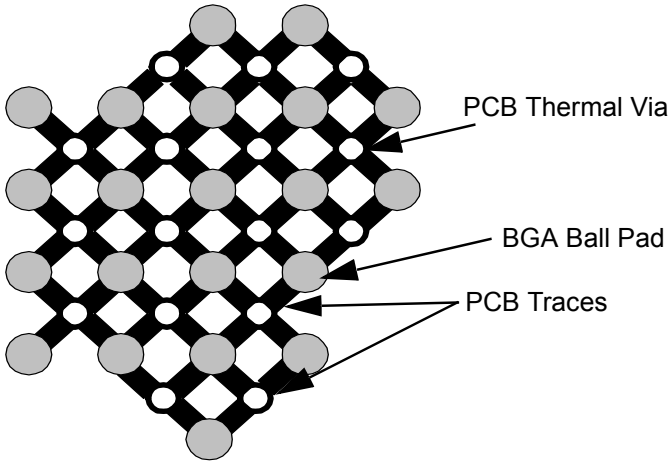


Figure 10: Thermal Via Layout

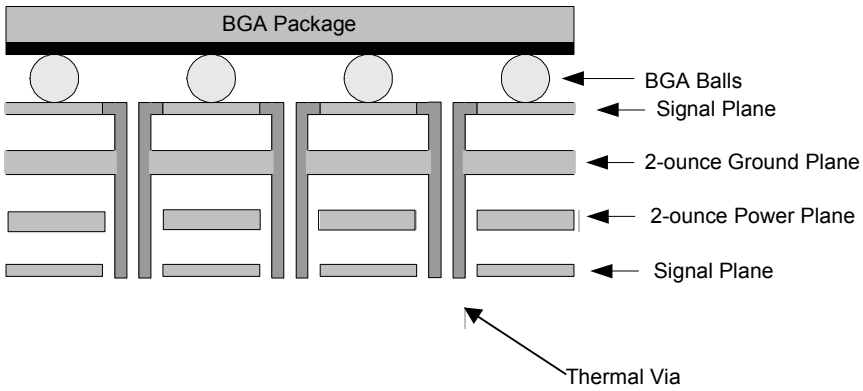


Figure 11: Thermal Ground Plane Connections

When connecting these thermal vias to ground planes, it is advisable not to use thermal-relief connection traces, as these are designed to prevent the flow of heat through the PCB. Instead, the thermal vias should have a solid connection to the traces and planes on each layer (see Figure 12: ”PCB Vias”, below).

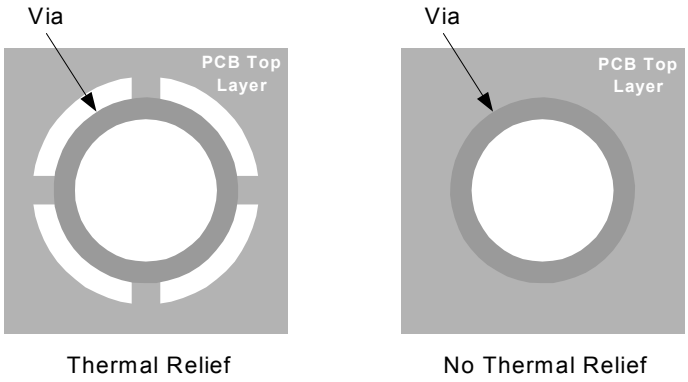


Figure 12: PCB Vias

Voltage Reference Pins Circuit

For proper operation, the VSC8221 must generate an on-chip band gap reference voltage at the REFFILT pin. For this, the following components are required for each VSC8221 in the system:

- 2.0kΩ reference resistor, 1% tolerance, 1/16 watt.
- Two 0.1uF capacitors, with 10% tolerance or better. NPO, X7R or X5R ceramic materials are all acceptable.

PCB Layout of Voltage Reference Pins Circuit

For best performance, special considerations for the ground connection of the voltage reference circuit are necessary to prevent bus drops which would cause inaccuracy in the reference voltage. This applies to the following elements:

- Ground connection of the 2.0kΩ reference resistor
- Ground connection of the 0.1uF reference capacitor

These ground connections should each be connected to a shared PCB signal trace, rather than being connected individually to a common ground plane. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitors and resistor should be placed as close as possible to the VSC8221. (see Figure 13: ”Voltage Reference Schematic”, below)

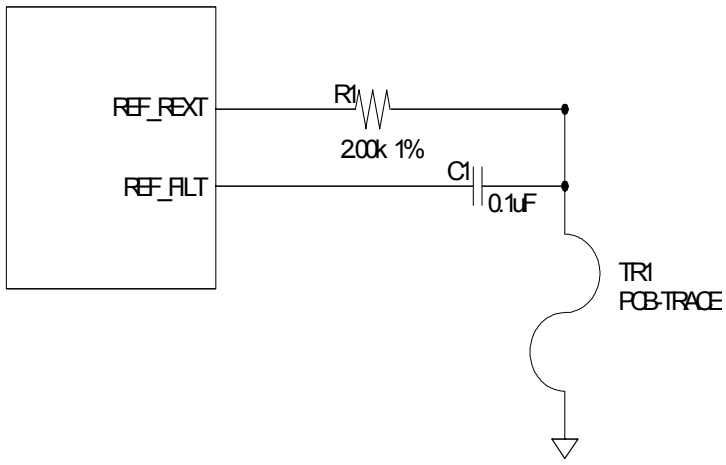


Figure 13: Voltage Reference Schematic

Document History & Notices

Revision Number	Date	Description
1.0.0	17 Sep 04	Initial Release