VSC8221 Evaluation Board

User Guide

VPPD-03471
Revision 1.0
December 2013

Vitesse

www.vitesse.com

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Revision History

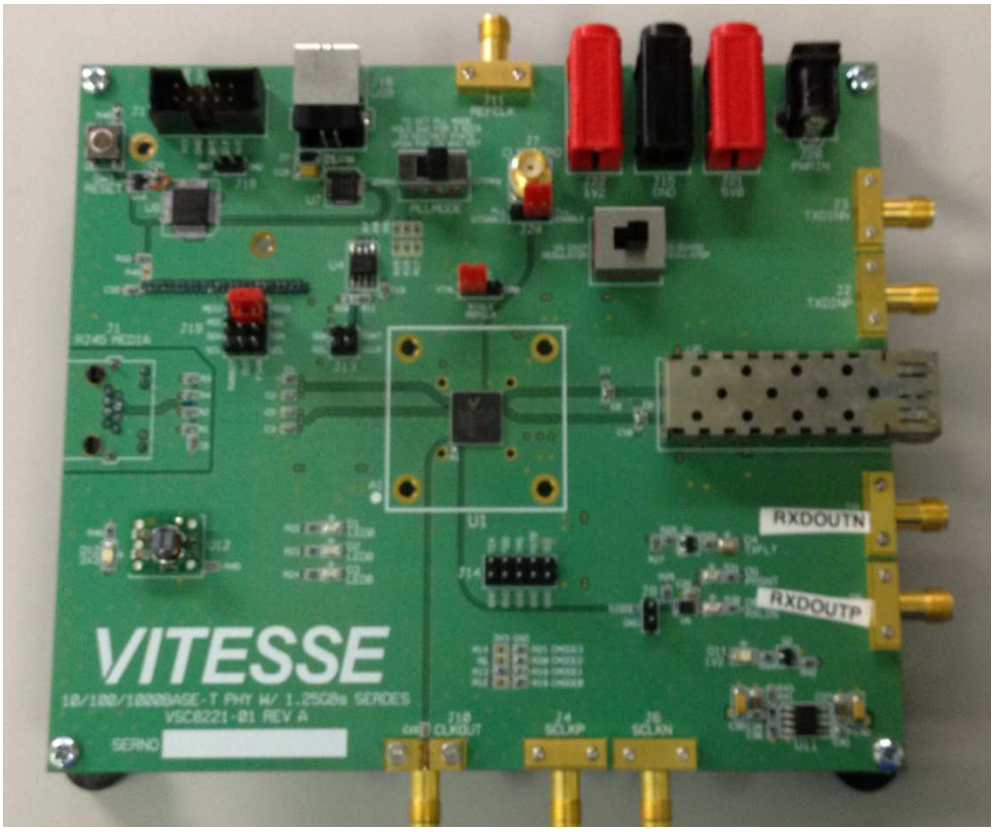
Revision	Date	Description
Rev 1.0	December 18, 2013	First release

1 Introduction

The VSC8221 device is a low-power, Gigabit Ethernet transceiver suited for Ethernet Switches with SGMII/SerDes MAC interfaces, Media Converter applications, and SFP/GBIC modules. The VSC8221 device also includes Vitesse's VeriPHY Cable Diagnostics feature.

This document describes the operation of the VSC8221 Evaluation Board (VSC8221EV). The Quick Start section describes how to install and run the graphical user interface (GUI) to fully control the evaluation board.

Figure 1. VSC8221EV



The following reference documents provide additional information about the operation of the VSC8221 evaluation board.

- VSC8221 Datasheet
  (https://www.vitesse.com/products/download.php?fid=190&number=VSC8221)
- VSC8221 Evaluation Board GUI
  (https://www.vitesse.com/products/download.php?fid=5158&number=VSC8221)
- VSC8221 Evaluation Board Schematics
  (https://www.vitesse.com/products/product.php?number=VSC8221)

2 General Description

The VSC8221EV provides the user a way to evaluate the VSC8221 device in multiple configurations. One RJ-45 connector is provided for the copper media interface. The MAC interface is provided via SMA connectors or alternatively through an SFP connector.

The VSC8221's internal registers are accessed via the MDIO bus from an external microcontroller driven by an external PC via USB. The accompanying GUI enables the user to read and write the device registers. Alternatively, the VSC8211EV also has the capability to configure the VSC8221 through an EEPROM or Rabbit microcontroller (not-provided).

The evaluation board has the option to use VSC8221's internal on-chip oscillator by connecting a 25MHz crystal to XTAL1 and XTAL2 or an external reference clock signal through the REFCLK SMA (J11).

2.1 Hardware Features

2.1.1 Power Connections

For convenience, the evaluation board runs off a single +5VDC power supply. On board DC-DC convertors create the +3.3VDC rail for the board and optional +1.2VDC rail. Power is supplied to the upper right corner of the board. Power can be applied either to the 5.5 x 2.1 mm barrel connector (J20) or the banana receptacles (J21 and J15). The slide switch (SW-4) selects between the external (on-board) and internal (on-chip) regulator option. J22 is an optional monitor point for the 1.2V rail. When powered by a bench top supply the board may draw up to 3A maximum, module included.

2.1.2 Copper Port RJ45 Connections

The RJ45 copper media PHY port (J1) uses a generic RJ45 jack with a discrete Pulse H5008 magnetic transformer.

2.1.3 SFP or SMA SGMII MAC Interface

The default MAC interface is provided through an SFP port connector. When using the SFP port, the SigDet polarity must be swapped in the VSC8221. See register 19E.0. Note that the transmit disable signals (TXDIS) are connected to ground, thus the laser is always turned on.

An optional MAC interface through SMA connectors may be enabled by removal and re-soldering the AC coupling caps (C7–C10) from horizontal to vertical position.

2.1.4 Switches

There are two switches on the board:

- SW4 to select between utilizing a +1.2V internal regulator or external regulator. The default option for the board is to use the external regulator.
- SW2 allows the user to select the mode of the EECLK/PLLMODE pin. In the on position a logic high voltage (pull-up resistor) configures the device for a 125MHz reference clock while a logic low voltage (pull-down resistor) selects a 25MHz reference clock option. This is a momentary ON switch which requires the user to hold it in the on position for 3 seconds during board power up or device reset.

2.1.5 Taitien 25MHz Crystal

The evaluation board is shipped configured to use the VSC8221's internal on-chip oscillator. The jumper on J12 should be installed in the XTAL (left) position, and the jumper on J24 should be installed in the PLL enable or VCC (right) position.

Note Review the required action for SW2 mentioned above.

2.1.6 External RefClk Option

The user may choose to provide an external PHY REFCLK via the SMA connector (J11). The user must configure the device by installing a jumper on J24 in the PLL disable or ground (left) position and installing a jumper on J12 in the SMA (right) position.

2.1.7 Silabs Microcontroller

A Silabs F340 microcontroller is included to facilitate a software interface to the registers on the VSC8221 through a USB port.

2.1.8 EEPROM Option

The user may choose to configure theVSC8221 via an EEPROM load. In order to program the EEPROM properly, pull-up or pull-down resistors must be configured for either R7 - R9 or R15 – R17. Please refer to Section 19 of the datasheet regarding to EEPROM programming requirement.

2.1.9 CMODE Pins

On the lower center of the board, there is an option to change the CMODE pin pull-up or pull-down resistors, R6, R12 – R14 and R18 – R21. Please refer to Section 18 of the datasheet for the detail on how to program the desired operating condition parameters

through the CMODE configuration bits and how to choose the value of each CMODE pull-up or pull-down resistor.

2.1.10 CLOCKOUT SMA

The user should observe a 125MHz output clock through this SMA if the internal PHY PLL is operating properly.

2.2 Software Requirements

The VSC8221 GUI can be loaded on to any PC or laptop that complies with the following requirements:

1. The PC must run a recent version of MS-Windows. According to the Microsoft website, the following operating systems can run .NET based applications:
   - Windows 2000
   - Windows XP
   - Windows Vista
   - Windows-7

Note The GUI may be slower when run on Windows 2000 operating system.

2. Hardware requirements must be considered when deploying/installing .NET applications. The minimum hardware requirement for a system running a .NET application is a Pentium 90MHz with 32 MB of RAM. For best performance, a newer system is recommended along with a minimum of 1 GB of RAM.
3. If the .NET Framework 2.0 is not already installed, it may be obtained from the following link: http://www.microsoft.com/downloads/details.aspx?FamilyID=0856EACB-4362-4B0D-8EDD-AAB15C5E04F5&displaylang=en

3 Quick Start

3.1 Board Configuration

Prior to powering the board, ensure that the jumpers and switches are in the following positions.

Table 1. Switch and Jumper Configuration

Switch/Jumper	Position
J19 (MDC)	Jumper installed connecting F340 MDC to DUT MDC
J19 (MDIO)	Jumper installed connecting F340 MDIO to DUT MDIO
J14 (TRSTB)	Jumper installed connecting to GND. This is not required when R48 is installed.
J12 (XTAL1/REFCLK)	Jumper installed connecting center pin to XTAL.

Switch/Jumper	Position
J24 (PLL ENABLE/DISABLE)	Jumper installed connecting center pin to PLL ENABLE.
SW2	Hold in the left position during power-up and reset.
SW4	Slide to the left to use the on-chip regulator.

3.1.1 Power Up

Provide +5VDC to the board by plugging in the power cable (included in the kit) to J20. Two green LEDs should illuminate: D12 on the left side of the board indicating +3.3VDC present, and D11 on the right side of the board indicating +1.2VDC present.

3.1.2 Clock and Reset

Power must be applied and the clock (either 25MHz or 125MHz) must be active at the correct frequency for the prescribed period of time in the datasheet before the RESETB pin is released. PLLMODE and OSCDISB pins are sampled during the device power-up or on assertion of RESETB pin.

The board will be shipped configured for use of the 25MHz crystal thus OSCDISB must be pulled up and PLLMODE must be pulled down during power-up or assertion of RESETB by setting J24 to the PLL enable position and holding SW-2 in the 25MHz position upon power-up.

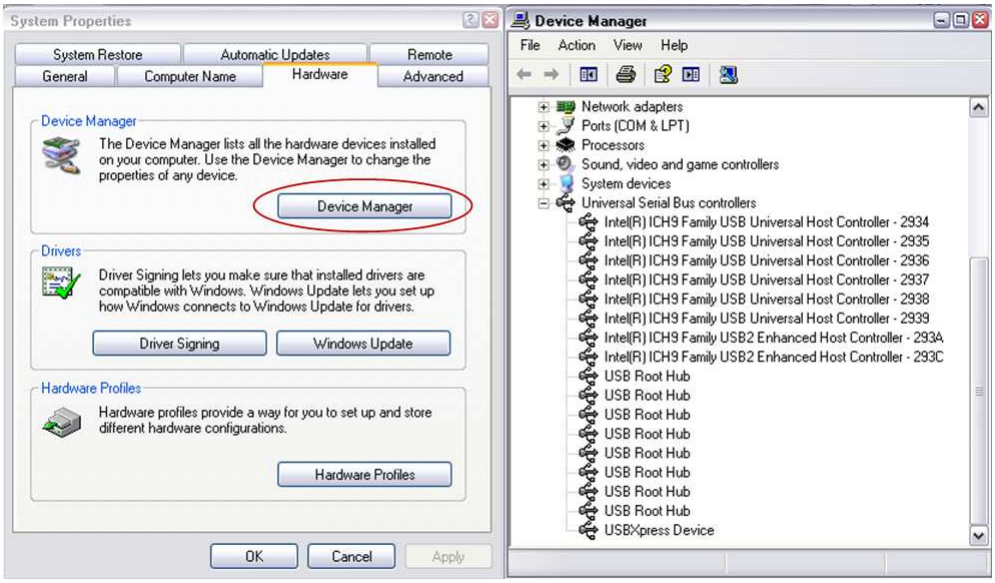
3.2 GUI and Driver Installation

Download the VSC8221EV GUI from Vitesse's website onto a PC that has a USB port. Install the GUI by launching the setup.exe file. Once installed, connect the USB cable between the USB port of the PC and the USB connector (J16) on the evaluation board. Ensure the MDIO and MDC jumpers are properly placed from DUT to F340 on J23 to establish the connection between the VSC8221's SMI pins and the SiLab F340.

USB communication is assisted by the Silabs USBXpress® drive. If not present on the PC, the user will need to download the USBXpress Development Kit from the Silicon Labs website (URL: http://www.silabs.com/products/mcu/Pages/USBXpress.aspx). Follow the installation directions after downloading the development kit.

To ensure the USBXpress driver is installed and properly recognizing the evaluation board, go to Control Panel and click on System>Hardware>Device Manager, and inspect the Universal Serial Bus controllers listed to see if "USBXpress Device" appears. Figure 2 shows that the PC recognizes that a USBXpress Device is connected.

Figure 2. USBXpress as Seen From the Device Manager Window



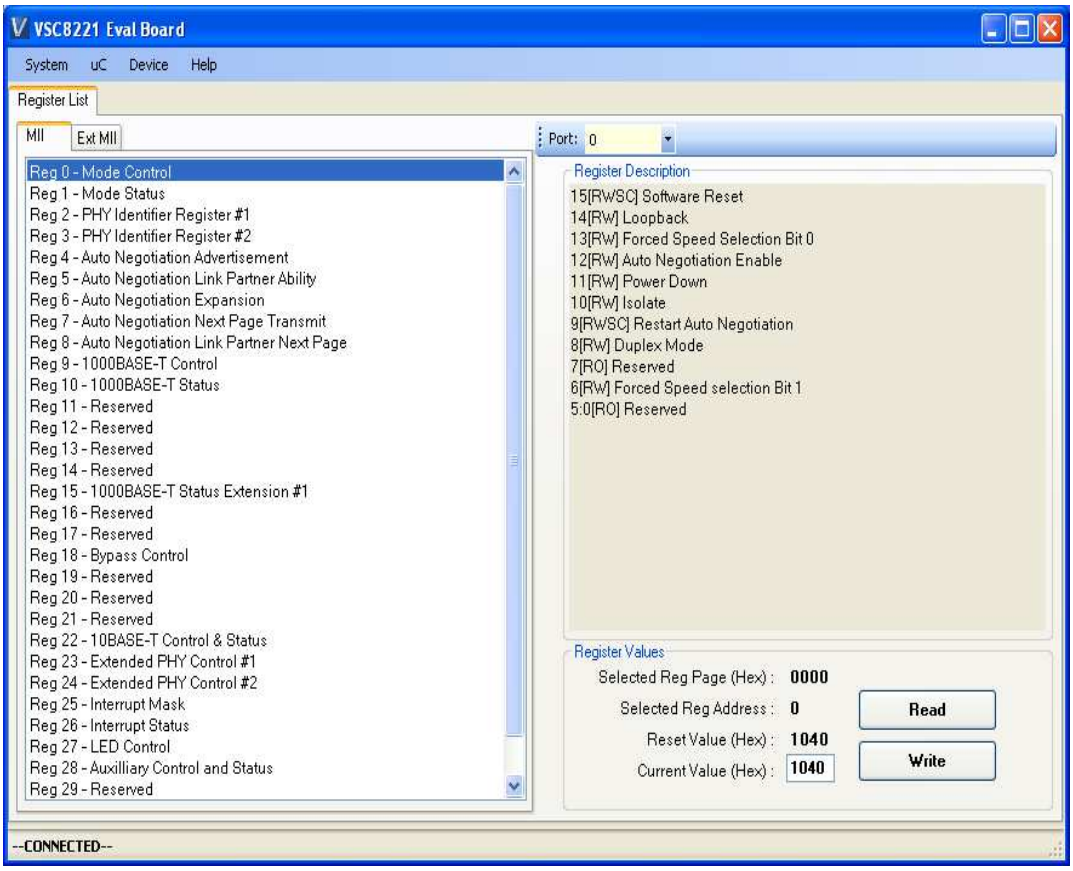
3.3 Using the GUI

Launch the GUI either by clicking on the Desktop shortcut or clicking on the "Start – Programs – Vitesse Semiconductor Corp - VSC8221_Evaluation_System" icons. The initial window will detect the attached USB devices automatically. Figure 3 shows a typical EVB Connection window.

Figure 3. Connection Window

The EVB serial number should appear. If not, click on "Scan For USB Devices." Select that EVB serial number then click "Launch GUI". The Register List window will appear as shown in Figure 4.

Figure 4. Register List Window



Verify that the device is up and running by reading MII Register 0. It should read back 0x1040. Reading back "0000" or "FFFF" (all 0's or all 1's) indicates a problem.

To read or write the extended MII registers click on the ExtMII tab.

An initialization script may be used to configure multiple VSC8221 registers. The initialization script is simply a text file which contains a list of registers to be written. Select the Device item on the top pull down menu area and click on Load-All-Registers option. A pop-up window will appear. Navigate to and select the desired script to be loaded.

As per Section 31.1 of the datasheet, there are a number of internal registers that must be changed from their default value during device initialization. Use this method to initialize the device by loading "vsc8221_workaround31_1.txt" included in the GUI package under the Script/ directory. GUI Setup

3.4 Test Cases

3.4.1 CAT5 to 802.3z Serdes with Clause 37 AutoNeg Detection

After power-up or reset, the VSC8221 will operate at CAT5 to 802.3z Serdes with clause 37 Auto Negotiation Detection mode. An SFP loopback module enables MAC side SGMII loopback. 1G Ethernet received by the VSC8221 RJ-45 port is routed through the VSC8221 and looped back via SGMII through the SFP Electrical Loopback module.

1. Set up the copper Ethernet traffic source (e.g., IXIA or Smartbits)
2. Connect an Ethernet cable to an RJ-45.
3. Plug in a SFP loopback module.
4. Monitor the link-up bit in MII Register 1, bit 2 (MII 1.2), read twice to update. Traffic should now be flowing.

3.4.2 CAT5 to SGMII with Modified Clause 37 AutoNeg Disabled

To configure the device for Clause 37 Auto-negotiation disabled, perform these steps:

1. Set up the copper Ethernet traffic source (e.g., IXIA or Smartbits)
2. Connect an Ethernet cable to an RJ-45.
3. Plug in a SFP loopback module.
4. Write 0xBA20 to "MII Register" (Port 0) Reg 23 (Extended PHY Control #1).
5. Write 0x9040 to "MII Register" (Port 0) Reg 0 (SW Reset for PHY Control setting to take effect).
6. Monitor the link-up bit in MII Register 1, bit 2 (MII 1.2), read twice to update. Traffic should now be flowing.

3.5 Useful Registers

3.5.1 Ethernet Packet Generator

ExtMII 29E is the Ethernet Packet Generator register. Refer to datasheet for configuration options.

A bad-CRC counter is in ExtMII 23.7:0. This counter will be saturate at 0xFF and is cleared when read.

3.5.2 Far-End Loopback

When MII Register 23 bit 3 is set to 1, it forces incoming data from a link partner on the media side to be retransmitted back to the link partner on the media interface.

3.5.3 Near-End Loopback

When MII Register 0 bit 14 is set to 1, the transmit data (TDP/TDN) on the MAC side is looped back onto the receive data (RDP/RDN pins) to the MAC.

4 Additional Information

For any additional information or questions regarding the devices mentioned in this document, contact your local sales representative.