SimpliPHY Synchronous Ethernet PHY Applications

Application Note

Subject to Change

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Contents

Document History

The following table lists the history of this document.

Table 1. Document History

Rev	Date	Description
01-00	07 Mar 2007	Initial Document Release

1 Introduction

The growth of Ethernet in telecom applications has created a demand for Ethernet PHYs capable of supporting Synchronous Ethernet. This application note will assist a system or high-speed board designer in determining which SimpliPHY device to implement into their design to support this feature.

1.1 Audience

The target audiences for this document are system or high-speed board designers determining which SimpliPHY device to implement into their Synchronous Ethernet design.

1.2 References

1.2.1 Vitesse Documents

- Datasheets are available for the VSC8211, VSC8224, VSC8244, VSC8601, VSC8641

1.2.2 IEEE Standards

- IEEE802.3 - CSMA/CD Access Method and Physical Layer Specification

1.3 Terms and Abbreviations

Table 2. Terms and Abbreviations

Term	Explanation
MAC	Media Access Control
MDI	Media Dependent Interface
PHY	PHYsical layer device
PLL	Phase Lock Loop
RGMII	Reduced Gigabit Media Independent Interface
SFP	Small Form-factor Pluggable
SIGDET	SIGnal DETect

2 Synchronous Ethernet

For the past decade, with the emerging prominence of Ethernet in telecommunications networks, carriers have been evolving their legacy circuit-switched systems to Ethernet packet-based systems. Traditionally, circuit-switched networks distributed a high quality clock source throughout the network in order to synchronize voice communications. Packet based networks, which were originally introduced to handle asynchronous data such as files, images and emails, did not require such restrictions to a master clock. However, the need for a method to synchronize these networks is becoming a specific requirement for carriers.

Synchronous Ethernet networks allow service providers to deliver all services over a single, converged Ethernet link. The availability of a reference timing signal with proper phase stability and frequency accuracy characteristics allows operators to migrate to a next-generation packet architecture supporting time-sensitive applications such as cellular, circuit emulation services, streaming video and VoIP.

Vitesse has Gigabit and 10 Gigabit Ethernet PHY solutions that enable system vendors to develop network equipment with sychronization aspects in accordance with ITU-T Recommendation G.8261/Y.1361. This application note discusses solutions that use the Gigabit Copper PHY Ethernet physical layer to provide reference timing signal distribution over packet networks. The solutions can offer a method for OEM vendors to provide Master and Slave timing capability on these same links.

3 Vitesse PHYs for Master Timing

A block diagram of a Vitesse PHY in master timing mode is shown:

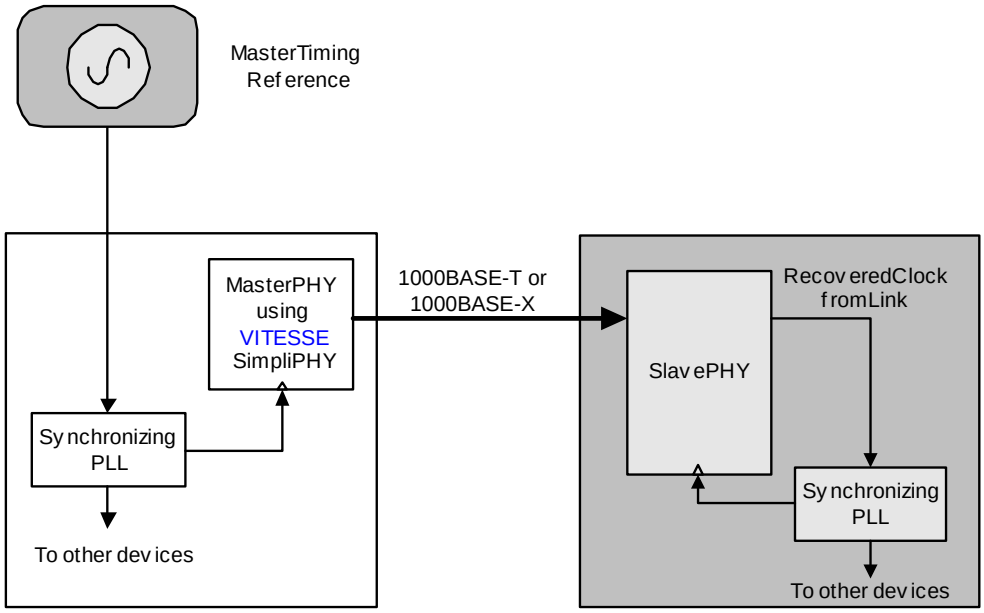

Figure 1. Master Timing Using a Vitesse SimpliPHY Device

In order for the PHY to be the master timing source in Ethernet applications, such as a Metro Ethernet appliance, it must be able to connect its reference clock input to the output of a PLL device that is capable of operating at the frequencies common to what is distributed in the system box. This can present a challenge as this requires a synchronizing PLL to connect directly to the internal PLL of the Gigabit Ethernet PHY. Vitesse has done testing with various PLLs. A PLL being tested was connected to the input clock pin of a PHY in order to allow the PHY to become the master timing source for both 1000BASE-T copper and 1000BASE-X fiber links. This testing showed that the slave PHY was able to track to the timing source of the master PHY in this Synchronous Ethernet application.

In order for the PHY to become the master timing source, the user must configure Register 9 of the master PHY to auto-negotiate to "Master Timing". The slave should be configured in a similar manner to auto-negotiate to "Slave Timing".

4 Vitesse PHYs for Slave Timing Recovery

A block diagram of a Vitesse PHY in slave recovery timing mode is shown:

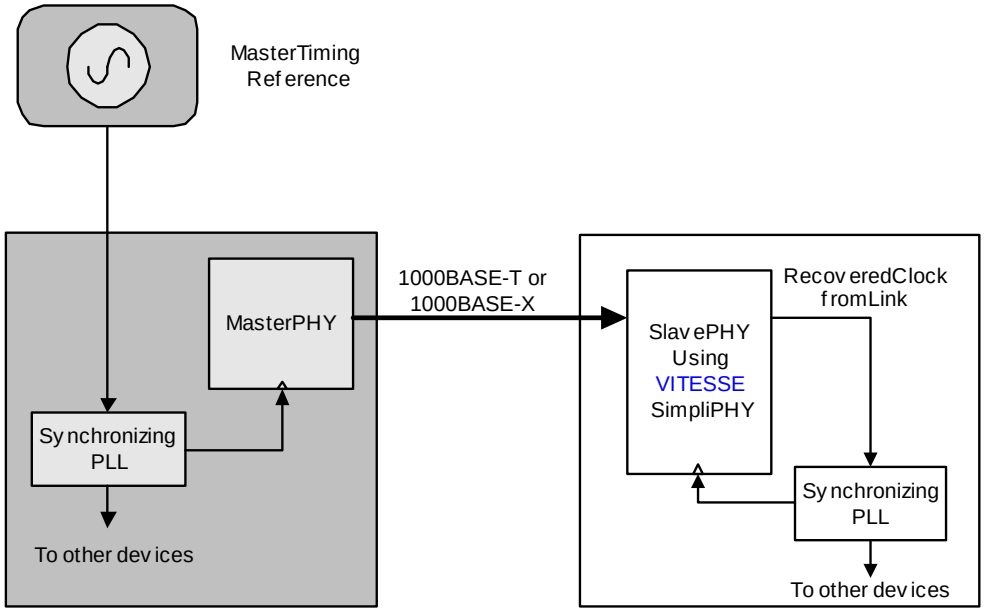

Figure 2. Slave Timing Recovery using a Vitesse SimpliPHY Device

The recovered clock from an incoming packet Ethernet signal is feed into an external synchronizing PLL, which can produce a low jitter reference signal that is traceable to the primary reference clock. In order for the PHY to be the slave timing recovery source, it must be able to connect the recovered clock coming off the PHY to the input of a PLL device that is capable of operating at the frequencies common to what is distributed on the system box. Vitesse has done testing with various PLLs. The PLL being tested was connected to the output recovery clock pin of several PHYs (including the VSC8601, VSC8641, VSC8211, VSC8224, VSC8224). The PHYs successfully performed slave timing recovery on both copper and fiber links. The slave PHY was able to track to the timing source from the master PHY when in this application.

In order for the PHY to become the slave timing recovery source, the user must configure Register 9 of the slave PHY to auto-negotiate to "Slave Timing". The master should be configured in a similar manner to auto-negotiate to "Master Timing". The recovery clock is then extracted from the RGMII RX_CLK pin (CLKOUTMAC pin on the VSC8211) when the PHY is restricted to "Slave Timing" [see Figure 3].

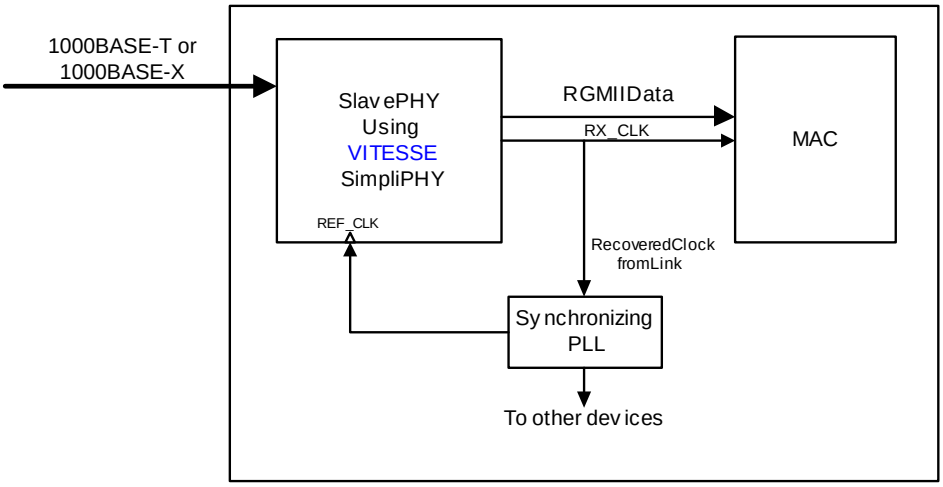

Figure 3. Slave Timing Recovery Using the RGMII Interface

5 Multi-port Vitesse PHYs in Master and Slave Timing Recovery

A block diagram of a multi-port Vitesse PHY in both master and slave recovery timing mode is shown in Figure 4.

Most hardware OEM vendors planning on supporting Synchronous Ethernet plan to implement several Gigabit Ethernet PHYs that are capable of being either master or slave timing recovery ports. This present a difficult challenge since one port of a multi-port PHY that is recovering the master clock from a main source has to simultaneously pass this clock out onto the other ports of its PHY so that these ports can be the master timing for another Ethernet box further down the path of the network. The resulting architecture is a mixture of both master and slave clock recovery and the PLL receiving the recovery clock must feed the same PHY. Vitesse has done testing with various PLLs connected in this manner using the VSC8224 and VSC8244, and have been successful in both receiving and transmitting timing. Data was also passed through this application and all links show error free operation. The two slave PHYs downstream from the Master timing source were able to track to the master timing clock's frequency.

For implementing this multi-port application, the previous design implementation notes for master and slave PHYs must both be followed.

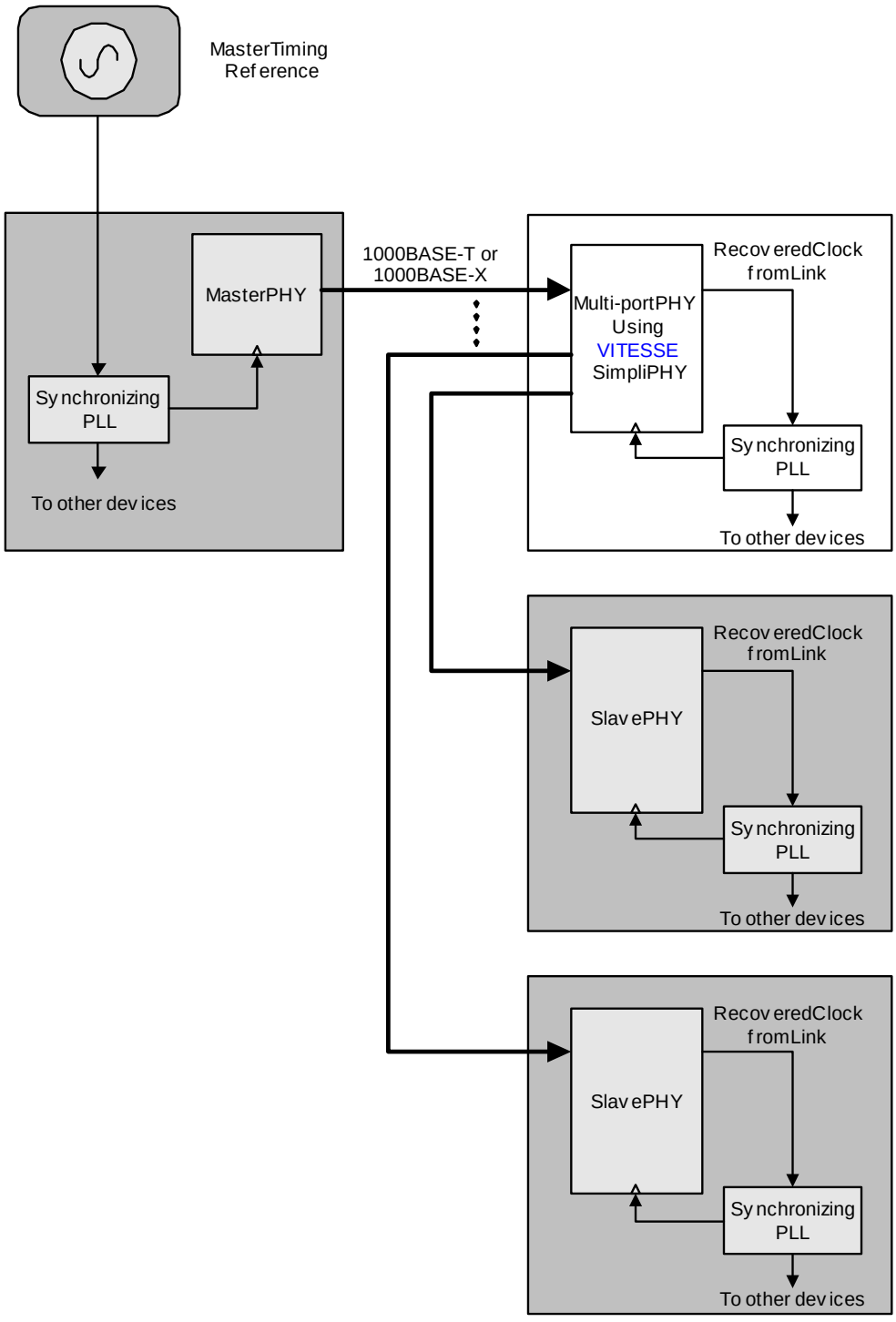

Figure 4. Master and Slave Timing Recovery Using a Multi-port Vitesse SimpliPHY Device