PD701xx/PD702xx

Application Note

Design for PD System Surge Immunity

June 2018

Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 was published in June 2018. The following is a summary of changes in revision 2.0 of this document.

- The format of this document was updated to the latest template.
- The immunity requirements (see page 3) and surge protection application circuit (see page 7) were updated in this publication.

1.2 Revision 1.21

Revision 1.21 was published in July 2017. The following is a summary of changes in revision 1.21 of this document.

- Fixed typo in TVS p/n in Table 3 (see page 6).

1.3 Revision 1.2

Revision 1.2 was published in July 2017. The following is a summary of changes in revision 1.2 of this document.

- Protection circuit for PD70224 and components list were added.
- Updated Table 3 (see page 6) and Figure 1 (see page 4) with note per IEC/EN 61000-4-5 Ed.3.

1.4 Revision 1.1

Revision 1.1 was published in February 2017. The following is a summary of changes in revision 1.1 of this document.

- Clarified test conditons and added test setup for shielded cables.

1.5 Revision 1.0

Revision 1.0 was published in September 2016. It was the first publication of this document.

2 Introduction

This document provides a detailed design guide to sustaining high voltage or current surges per typical immunity requirements in PoE PD systems using Microsemi, controllers PD701xx and PD702xx.

The following table lists different device types of PD system surge immunity.

Table 1 • PD System Surge Immunity Design

Device Type	Power Capability	Integrates PWM
PD70100	IEEE 802.3at Type 1 (IEEE 802.3 af)	No
PD70101	IEEE 802.3at Type 1 (IEEE 802.3 af)	Yes
PD70200	IEEE 802.3at Type 2	No
PD70201	IEEE 802.3at Type 2	Yes
PD70210/A	IEEE 802.3at Type 2 (2/4 pair) HDBaseT (95W)	No
PD70211	IEEE802.3at Type 2 (2/4 pair) HDBaseT (95W)	Yes
PD70224	IEEE802.3at Type 2 (2/4 pair) HDBaseT (95W)	N/A

Surge immunity is a basic feature required within telecommunication systems to increase system reliability when exposed to a surge event. Surge protection is usually divided into two protection stages.

- Primary protection deals with high energy surges and is usually located between Equipment Under Test (EUT) and an external cable subjected to the surge event. However, it can also be implemented at the EUT frontend. It is used primarily for outdoor cable installations.
- Secondary protection deals with lower surge energies and is usually located within the EUT frontend. It is used mainly for indoor cable installations.

None of the protection stages is intended to protect from direct lightning strike events. They are intended to protect from common surge events occurring near the telecommunication line. This design guide will assist the designer to implement a primary protection mechanism for protection from indoor or outdoor surge events.

3 Immunity Requirements

Various agencies around the world define different surge voltage levels, source impedance, and maximum surge current. This document provides information only on IEC/EN 61000-4-5 (2014 Ed.3) and ITU-T K21, which are the most common surge immunity standards in PoE PD systems.

IEC 61000-4-5 states that due to the nature of unshielded wiring, coupling to symmetrical interconnection lines (twisted pairs) is always in common mode, that is between all lines to ground. However, ITU-T K.21 specifies for unshielded PoE lines a differential mode surge as well. Currently, IEEE 802.3 does not define the PoE surge requirements. It is up to the customers to choose what standard best fits their application.

For indoor applications, IEC 61000 4-5 specifies 1.2/50 µs-8/20 µs common mode surge waveform with voltage level 0.5 kV to 2.0 kV depending on installation class. However, some customers may choose meeting higher levels of protection, such as 4 kV, which are suitable for outdoors.

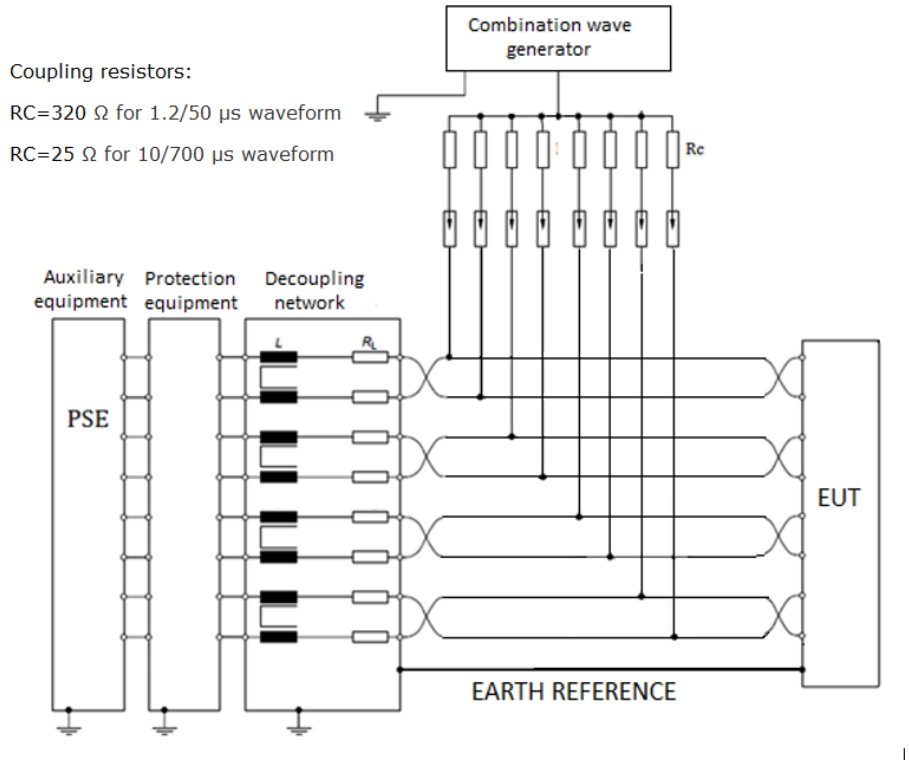
Common mode surge protection requires voltage limiting components that bridge the insulation between PoE domain and earth ground. The IEC/UL 60950-1 indicates that these limiters can be removed for insulation testing. However, subclause 6.1.2.1 of the standards also specifies minimum rated operated voltage of these limiters as a function of AC mains supply in the area where the equipment is installed unless the equipment qualifies for 6.1.2.2 exclusions. For a worldwide application this requires minimum operation voltage of the surge protectors over their expected life to be at least 360 V. Similarly, ITU-T now requires 500 VDC insulation test without removing any voltage limiters to verify the insulation is still good after the surge tests. For these reasons, in our common mode surge tests we used voltage limiting devices rated 500 VDC or above. A 100 m CAT5 cable is used as a decoupling network. The following table provides a quick summary of the analyzed test requirements, which are typical for indoor and outdoor applications.

Table 2 • Typical Telecom Surge Requirements

Number	Standard	Wave Shape	Level	Criteria	Type	Setup
1	EN 61000 4-5 (indoors)	1.2/50-8/20 µs 1.2/50-8/20 µs	±4 kV	A	All Lines to Earth	15 Ω internal plus 320 Ω + 90 V gas arrestor per line port On and port Off. See Figure 1 (see page 4).
2	EN 61000 4-5 (indoors > 300 m)	10/700 µs	±4 kV	A	All Lines to Earth	15 Ω internal plus 25 Ω + 90 V gas arrestor per line port On and port Off. See Figure 1 (see page 4).
3	ITU-T K21	1.2/50-8/20 µs	±600 V (basic test) ±1.5 kV (enhanced test)	A	Line to line	2 Ω internal plus 10 Ω port On and port Off. See Figure 2 (see page 5).
4	EN 61000 4-5 (shielded cable)	1.2/50-8/20 µs	±4 kV	A	Chassis to Earth	2 Ω internal plus 18 F port On and port Off. See Figure 3 (see page 5).

Figures 1 - 3 (see page 4) show test setups for common mode and differential mode surges on PoE lines.

Figure 1 • Example of Test Setup for Common Mode Surge in PoE PD Port



For 1.2/50 µs test the effective internal impedance of the combination generator in the following illustration is 2 Ω plus external resistors Rc=40 Ω × n per line, where n-number of lines. For 4-pair cable, (n=8) Rc=320 Ω. For 10/700 µs tests Rc=25 Ω.

Figure 2 • Example of Test Setup for Transverse/Differential Mode Surge on PoE PD Port

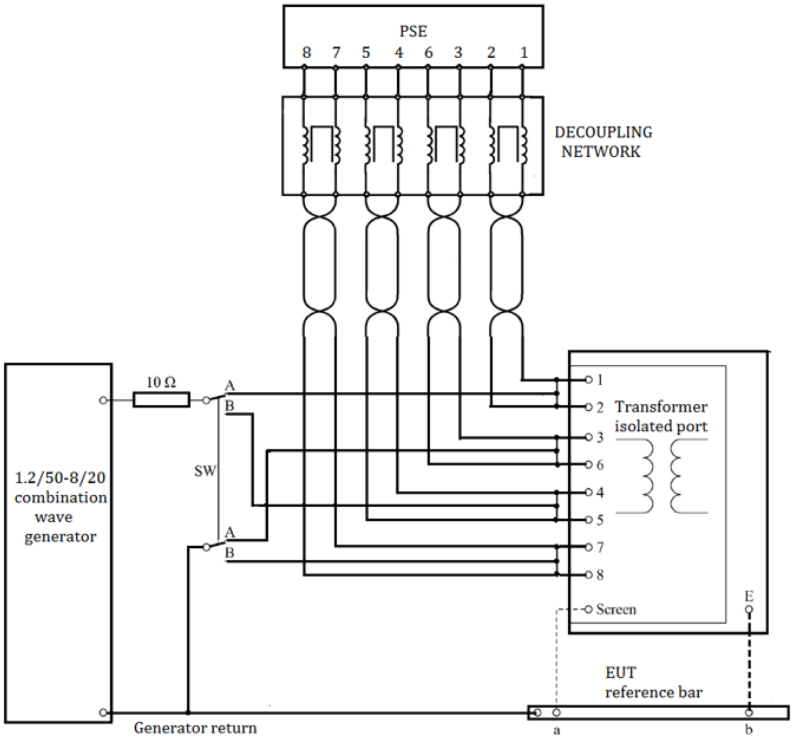
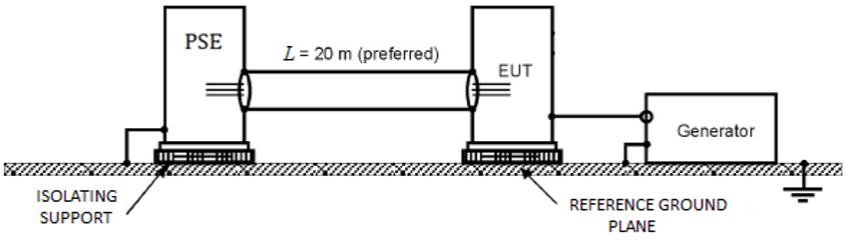


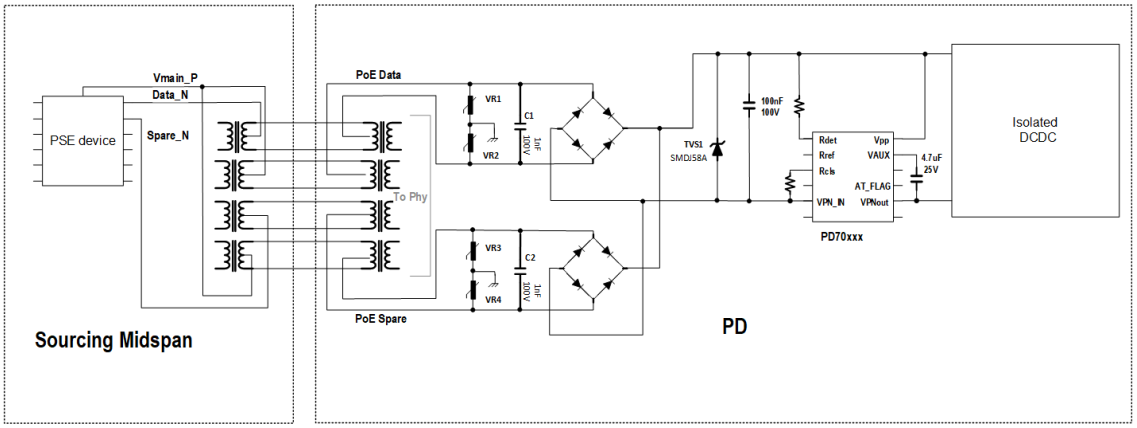
Figure 3 • Example of Test Setup for Surges Applied to Shielded Lines



4 Surge Protection Circuit Design

The following circuit allows immunity for the test levels in the following table (up to 4 kV common mode and 1.5 kV differential mode surges) tested with net amount of common mode capacitors up to 10 nF.

Figure 4 • Surge Protection Circuit



The parts in the following table may be replaced by equivalent.

Table 3 • Surge Protection Components per Port

Quantity	Reference	Description	Size	Manufacturer	
				Brand	Part Number
4	VR1-VR4	Varistor 385 VAC/505 VDC, 27 J peak pulse current	11.4 mm × 8.3 mm	Littlefuse	V385SM7
1	TVS1	TVS Diode 58 VWM 5000 W Uni-directional	SMD	Littlefuse	SMDJ58A
1	C1, C2	1 nF 100 V X7R	0603	Samsung	CL10B102KC8NNC

4.1 Surge Protection Circuit for Use With PD70224 Ideal Bridge

The following circuit allows immunity for up to 4 kV 1.2/50 µs-8/20 µs common mode surge per IEC 61000 4-5 tested with net amount of common mode capacitors up to 10 nF.

Figure 5 • Surge Protection Circuit for PD70224

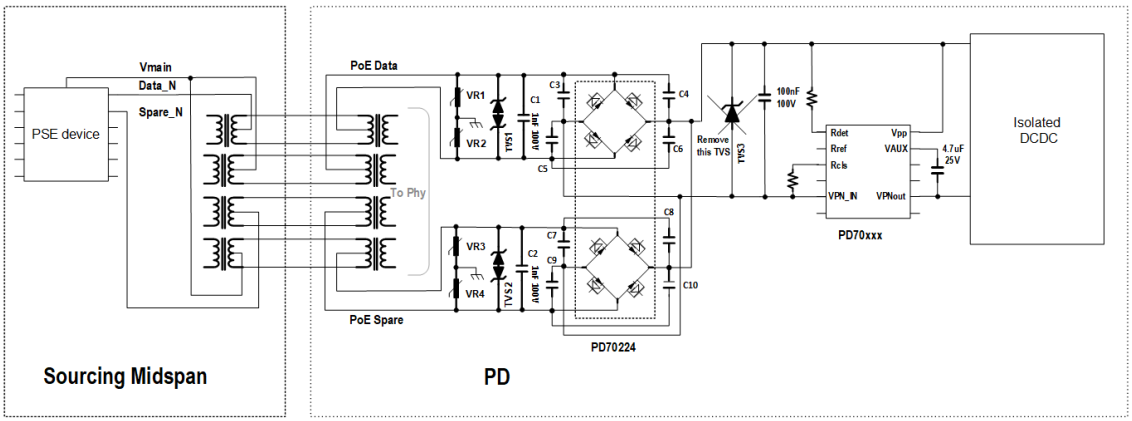


Table 4 • Surge Protection Components for PD70224 per Port

Quantity	Reference	Description	Size	Manufacturer	
				Brand	Part Number
4	VR1-VR4	Varistor 385 VAC/505 VDC, 27 J 1200 A Peak pulse current	144 mm disc	Epcos	B72214S2421K101
2	TVS1-TVS2	TVS Diode 58 VWM 5000 W bi-directional	SMD	Littelfuse	5.0SMDJ58CA
2	C1, C2	1 nF 100 V X7R	0603	Samsung	CL10B102KC8NNNC
8	C3-C10	10 nF 100 V X7R	0603	TDK	C1608X7R2A103K080AA

Note: Do not use PD70224 in applications that require a differential mode surge protection.

4.2 Avoid Additional Earth Ground Return Passes for Surge Current

Common mode TVS's divert surge currents to the earth ground. Thus, preventing them from flowing through the PD circuit. It is important to minimize additional low-impedance passes for the surge current downstream the rectifier bridge. Such additional pass can be created by common mode capacitors in EMI filter or by a wall adapter with an internal output common mode capacitor or surge suppressor. When such adapter is connected after PD chip, a portion of surge current will flow to the adapter output through the PD chip's internal FET and can cause its damage. If a PD system has to provide surge immunity when both PoE and adapter are connected, the adapter has to be selected either with no TVS and capacitors from its DC output to earth ground, or without ground prone in its input AC line cord.

Another example of unwanted additional ground return pass is a non-isolated PD-PSE system in which PD frontend feeds PSE through a boost converter. In such a system, when a surge voltage is injected on either the PD or PSE connector, the surge current will flow through common analog return of PD and PSE and may damage the circuit. Therefore, if PD system is intended to power a PSE, there should be an isolation between the two. Such isolation can be provided by using a flyback converter instead of boost. The compliance of the protection circuits in Figure 4 (see page 6) and Figure 5 (see page 7) was tested with net amount of all common mode capacitors up to 10 nF and without auxiliary power sources.

4.3 Layout Considerations

Care should be taken on PCB layout with respect to surge immunity.

- Keep chassis traces close to RJ45 or ground screws (if any) and do not penetrate PoE environment.
- Keep at least 80 mil creepage between chassis and PoE circuitry.
- Keep surge protection components as close as possible to RJ45 or chassis connection to minimize high current loops.
- Make connections of surge protectors by short heavy traces capable of withstanding surge currents.
- Do not use these traces for connecting other components.

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